REMARKS

Claims 1-18 are present in the application.

Claims 1-6 and 8-18 are rejected as unpatentable over applicant's disclosed prior art (Figure 6) in combination with SUMIKAWA (JP 2000-183531) and claim 7 is rejected over SUMIKAWA and applicant's disclosed prior art in view of LAU (Chip Scale Package article). These rejections are respectfully traversed.

Applicant claims priority from Japanese Application No. 2000-140174 filed May 12, 2000. The verified English translation of the foreign priority application is submitted herewith to perfect the claim of priority. Since the Japanese filing date, and hence the latest possible date of invention, precedes the June 30, 2000 publication date of SUMIKAWA, SUMIKAWA cannot be used as a prior art reference.

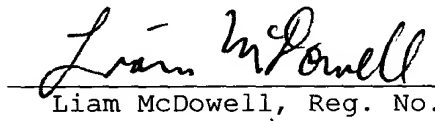
The SUMIKAWA reference is unavailable as prior art under §102(b), as the June 30, 2000 publication date falls less than one year prior to the May 3, 2001 U.S. filing date of the present application. Accordingly, the reference is unavailable, if at all, only under §102(a).

Since all the claims were rejected using SUMIKAWA as a reference, and SUMIKAWA is not a valid prior art reference, the claims should be allowable.

Reconsideration and allowance are respectfully requested.

Respectfully submitted,

YOUNG & THOMPSON



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APPENDIX:

The Appendix includes the following item:

- a verified English translation of foreign priority document

CERTIFICATE OF VERIFICATION

I, Yasuyuki Hata of c/o Saito & Hata International Patent Office, Akasaka-taisei Bldg., 1-18, Akasaka 1-chome, Minato-ku, Tokyo, Japan, hereby certify that I am the translator of the document attached and I state that the attached document is a true and complete translation to the best of my knowledge and belief of Japanese Patent Application No. 2000-140174 filed on May 12, 2000.

Dated this 15th day of August, 2003

Signature of translator Yasuyuki Hata

Yasuyuki Hata

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【 List of Filed Documents】

【 Name of Paper】 Specification 1

【 Name of Paper】 Drawing 1

【 Name of Paper】 Abstract of Disclosure 1

【Number of General Power of Attorney】 9710078

【Necessity for Proof 】 yes

【Document Name】 SPECIFICATION

【Title of the Invention】 ELECTRODE STRUCTURE OF A CARRIER SUBSTRATE OF A SEMICONDUCTOR DEVICE

【Scope of claim for patent】

1. An electrode structure of a carrier substrate of a semiconductor device for solder-bonding the semiconductor device to a main substrate, wherein an electrode having a recess in a central area of said electrode and a circumferential wall surface surrounding said recess, and said electrode further having, on said circumferential wall, a through portion connecting said recess of said central area to an outer area portion outside of said wall surface.

2. An electrode structure of the carrier substrate of the semiconductor device according to claim 1, wherein said electrode is hemispheric configuration having a flange portion and having a concentric hemispheric hollow portion thereinside, wherein said hemispheric portion of said electrode being fitted into a hemispheric recess provided on an outer surface of said carrier substrate of said semiconductor device, and said electrode being fixedly attached to said carrier substrate so that said flange portion abuts said outer surface of said carrier substrate.

3. An electrode structure of the carrier substrate of the semiconductor device according to claim 2, wherein said through portion passing through between said recess and said outer area portion out side of said wall surface being at least one slit portion provided in said flange portion and in said wall surface of said electrode adjacent to said flange portion.

4. An electrode structure of said carrier substrate of said semiconductor device according to claim 1, wherein said electrode

is cylindrical having a flange portion and having a concentric cylindrical hollow portion thereinside, said cylindrical portion of said electrode being fitted into a cylindrical recess provided on an outer surface of said carrier substrate of said semiconductor device, and said electrode is fixedly attached to said carrier substrate so that said flange portion abuts said outer surface of said carrier substrate.

5. An electrode structure of said carrier substrate of said semiconductor device according to claim 4, wherein said through portion passing through between said recess and said outer area portion out side of said wall surface being at least one slit provided in said flange portion and in said cylindrical wall surface of said electrode adjacent to said flange portion, said slit being extended from said flange portion to a position close to a bottom thereof.

6. An electrode structure of the carrier substrate of the semiconductor device according to claim 1, wherein a package of said semiconductor device is of a BGA (ball grid array) type.

7. An electrode structure of the carrier substrate of the semiconductor device according to claim 1, wherein a package of said semiconductor device is of a CSP (chip scale package) type.

【Detailed Description of the Invention 】

【Field of the Invention】

The present invention relates to an electrode structure of a semiconductor device for solder-bonding the semiconductor device to a main substrate.

【Prior Arts】

In order to make personal home electric appliances such as a portable telephone, a video camera, and a personal computer small,

compact, lightweight, the package of a semiconductor device has been changed from an LSI package having a gull-wing type lead electrode to a BGA (ball grid array) type or a CSP (chip scale package) type which are compact, lightweight packages. FIG. 5 is an outward view of a BGA type package semiconductor device, and (a) is a side view and (b) is a bottom view. FIG. 6 is a partial side view of a state where the BGA type package semiconductor device of FIG. 5 is bonded to a main substrate. The semiconductor element which is mounted to a carrier substrate 502 and is not shown in the drawing is sealed in a package composed of a resin part 501 and the carrier substrate 502, and an external terminal of the semiconductor element is connected to an external part via a soldering land 503 that is an electrode grid-like arranged on the carrier substrate 502. A soldering land 602 is provided at a position corresponding to the soldering land 503 of the carrier substrate 502 of the semiconductor device in the main substrate 601 in which the semiconductor device is mounted and is bonded to the soldering land 503 of the semiconductor substrate via solder 603. Both soldering land 503 and soldering land 602 have cylindrical shapes with low heights, their upper faces are generally smooth flat faces, and the smooth upper faces of both lands are bonded across the solder 603.

【Problem to be solved by the Invention】

The interval of the lands becomes narrow and the areas of lands become small with miniaturization of a package, and thus a problem that the joint strength and the reliability of the lands by means of the solder become low has occurred.

It is an object of the present invention to provide an electrode structure of a carrier substrate of a semiconductor device in which

the strength and the reliability of the joint portion between an electrode of a semiconductor package and an electrode of a main substrate are improved.

【Means for solving the Problem 】

An electrode structure of a carrier substrate of a semiconductor device of the present invention is an electrode structure of a carrier substrate of a semiconductor device for solder-bonding the semiconductor device to a main substrate, wherein an electrode having a recess in a central area of said electrode and a circumferential wall surface surrounding said recess, and said electrode further having, on said circumferential wall, a through portion connecting said recess of said central area to an outer area portion outside of said wall surface.

The electrode may be hemispheric having a flange portion and has a concentric hemispheric face hollow portion thereinside, the hemispheric portion of the electrode may be fitted into a hemispheric recess provided on an outer surface in the carrier substrate of the semiconductor device, and the electrode may be fixedly attached to the carrier substrate so that the flange portion abuts the outer surface of the carrier substrate. The through portion connecting the recess to the outer portion of the wall surface, may be at least one slit provided in the flange portion and the wall surface of the electrode adjacent to the flange portion.

The electrode may be cylindrical having a flange portion and has a concentric cylindrical hollow portion thereinside, the cylindrical portion of the electrode may be fitted into a cylindrical recess provided on an outer surface in the carrier substrate of the semiconductor device, and the electrode may be fixedly attached to the carrier substrate so that the flange portion

abuts the outer surface of the carrier substrate.

The through portion provided in the electrode and connecting the recess to the outer portion of the wall surface may be at least one slit provided in the flange portion and the cylindrical wall surface of the electrode adjacent to the flange portion and the slit extending to a position close to a bottom of the cylindrical recess.

The package of the semiconductor device may be of a BGA type or a CSP type.

By forming a recess in a central area of the electrode, a joint area between a soldering land and solder increases, and the joint is three-dimensional. Further, since a through portion connecting the recess and the outer portion of the wall surface is provided, the air thereinside escapes, and solder becomes wet and spreads in the recess fully, whereby the same strength joint can be achieved by a small amount of solder and the interval between the carrier substrate and the main substrate can be narrowed

【Mode of operation】

It is an object of the present invention to improve the structure of a soldering land that is an electrode for improving the reliability of a solder joint portion of a semiconductor device and particularly to improve the structure of a soldering land in a ball grid array package (hereafter, BGA) and a chip size package (hereafter, CSP) of an LSI.

Next, embodiments of the present invention are explained referring to drawings. FIG. 1 is a schematic view showing an electrode structure of a carrier substrate of a semiconductor device of a first embodiment of the present invention, and (a) is a plan view, (b) is a side sectional view taken on the line A-A of (a),

and (c) is a side sectional view taken on the line B-B of (a). FIG. 2 is a partial side view of a state where the carrier substrate of the semiconductor device of FIG. 1 is bonded to a main substrate.

Referring to FIG. 1, a soldering land 103 that is an electrode of a carrier substrate 102 which was conventionally cylindrical is hemispheric having a hollow portion of a concentric hemispheric face thereinside and is provided with a flange portion in the circumferential portion thereof in the first embodiment, and the outer diameter of the flange portion corresponds to the outer diameter of the conventional cylinder.

Two slits 104 are provided in the flange portion and parts of a wall surface of the soldering land 103 adjacent to the flange portion for venting air. A hemispheric face recess is provided in the carrier substrate 102 toward an outer surface, and the soldering land 103 is fixedly attached to the carrier substrate 102 so that the soldering land 103 is fitted into the recess and the flange portion abuts the outer surface of the carrier substrate.

A semiconductor element which is mounted to the carrier substrate 102 and is not shown is sealed in a package composed of a resin part 101 and the carrier substrate 102, and an external terminal of the semiconductor element is connected to an external part via the soldering land 103 that is an electrode grid-like arranged on the carrier substrate 102.

As shown in FIG. 2, a soldering land 202 is provided at a position corresponding to the soldering land 103 of the carrier substrate 102 of the semiconductor device in the main substrate 201 in which the semiconductor device is mounted, and solder printing is implemented on the main substrate 201. Then, BGA and CSP having the hemispheric soldering land 103 having the recess

are mounted to the main substrate 201 so that the soldering land 202 of the main substrate 201 and the soldering land 103 of the BGA and the CSP corresponding thereto are matched.

Then, these are thrown into a reflow furnace for soldering, printed solder 203 is melted, and the solder 203 becomes wet and starts spreading over the soldering land 202 of the main substrate 201 and the soldering land 103 of the BGA and the CSP. Air stagnates in the recess of the soldering land 103 of the BGA and the CSP, and usually the air prevents the solder 203 from invading into the recess. However, in the first embodiment of the present invention, since the air inside the recess escapes via the slits 104 shown in FIG. 1, it becomes possible for the solder 203 to become wet and spread in the recess fully. When they are taken out from the reflow furnace, the solder hardens, and the soldering land 202 of the carrier substrate 201 is bonded to the soldering land 202 of the main substrate 102.

By changing the structure of the soldering land 103 from a conventional flat face to a recess, the solder joint area can be increased, and the reliability of the joint portion can be improved.

In the explanation above, although the shape of the soldering land 103 is hemispheric having a hollow portion of a concentric hemispheric face thereinside and is provided with a flange portion in the circumferential portion thereof, the shape may be cylindrical having a hollow portion of hemispheric face thereinside, and a slit for venting air may be provided.

Next, a second embodiment of the present invention is explained referring to drawings. FIG. 3 is a schematic view showing an electrode structure of a carrier substrate of a semiconductor device of the second embodiment of the present invention, and (a) is a

plan view and (b) is a side sectional view taken on the line C-C of (a). FIG. 4 is a partial side view of a state where the carrier substrate of the semiconductor device of FIG. 3 is bonded to a main substrate.

Referring to FIG. 3, a soldering land 303 that is an electrode of a carrier substrate 302 which was conventionally cylindrical is cylindrical having a concentric cylindrical hollow portion thereinside and is provided with a flange portion in the circumferential portion of the upper portion thereof in the second embodiment, and the outer diameter of the flange portion corresponds to the outer diameter of the conventional cylinder. This is a similar structure to a through-hole and can be formed by a similar manufacturing method. Two slits 304 are provided in the flange portion and in a wall surface adjacent to the flange portion and the slit extending to positions close to the bottom face thereof for venting air.

A cylindrical recess is provided in the carrier substrate 302 toward an outer surface, and the soldering land 303 is fixedly attached to the carrier substrate 302 so that the soldering land 303 is fitted into the recess and the flange portion abuts the outer surface of the carrier substrate.

A semiconductor element which is mounted to the carrier substrate 302 and is not shown is sealed in a package composed of a resin part 301 and the carrier substrate 302, and an external terminal of the semiconductor element is connected to an external part via a soldering land 303 that is an electrode grid-like arranged on the carrier substrate 302.

As shown in FIG. 4, a soldering land 402 is provided at a position corresponding to the soldering land 303 of the carrier substrate

302 of the semiconductor device in the main substrate 401 in which the semiconductor device is mounted, and solder printing is implemented on the main substrate 401. Then, the BGA and the CSP having the cylindrical soldering land 303 having the hollow portion are mounted to the main substrate 401 so that the soldering land 402 of the main substrate 401 and the soldering land 303 of the BGA and the CSP corresponding thereto are matched.

Then, these are thrown into a reflow furnace for soldering, printed solder 403 is melted, and the solder 403 becomes wet and starts spreading over the soldering land 402 of the main substrate 401 and the soldering land 303 of the BGA and the CSP. Air stagnates in the hollow portion of the soldering land 303 of the BGA and the CSP, and usually the air prevents the solder 403 from invading into the hollow portion. However, in the second embodiment of the present invention, since the air inside the hollow portion escapes via the slits 304 shown in FIG. 3, it becomes possible for the solder 403 to become wet and spread fully. When they are taken out from the reflow furnace, the solder hardens, and the soldering land 303 of the carrier substrate 302 is bonded to the soldering land 402 of the main substrate 401.

By changing the structure of the soldering land 303 from a conventional flat face to a cylinder having a hollow portion, the solder joint area can be increased, and the reliability of the joint portion can be improved.

【Effect of the Invention】

As described above, the present invention produces the following advantageous effects.

A first advantageous effect is that the strength and the reliability of a solder joint portion can be improved. This is

because the joint area between a soldering land and solder is increased and the joint is three-dimensional.

A second advantageous effect is that the height of mounting can be restrained since the amount of solder of the solder joint portion can be reduced. This is because the same strength joint can be achieved by a small amount of solder and the interval between the carrier substrate and the main substrate can be narrowed since the joint between the soldering land and solder becomes three-dimensional, and thus the solder invades the inside of the soldering land.

【BRIEF DESCRIPTION OF THE DRAWINGS】

FIG. 1 is a schematic view showing an electrode structure of a carrier substrate of a semiconductor device of a first embodiment of the present invention, and (a) is a plan view, (b) is a side sectional view taken on the line A-A of (a), and (c) is a side sectional view taken on the line B-B of (a);

FIG. 2 is a partial side view of a state where the carrier substrate of the semiconductor device of FIG. 1 is bonded to a main substrate;

FIG. 3 is a schematic view showing an electrode structure of a carrier substrate of a semiconductor device of a second embodiment of the present invention, and (a) is a plan view and (b) is a side sectional view taken on the line C-C of (a);

FIG. 4 is a partial side view of a state where the carrier substrate of the semiconductor device of FIG. 3 is bonded to a main substrate;

FIG. 5 is an outward view of a BGA type package semiconductor device, and (a) is a side view and (b) is a bottom view; and

FIG. 6 is a partial side view of a state where the BGA type

package semiconductor device of FIG. 5 is bonded to a main substrate.

【Explanation of Symbols used in this specification】

101, 301, 501	resin part
102, 202, 302, 502	carrier substrate
103, 303, 503	soldering land
104, 304	slit
201, 401, 601	main substrate
202, 402, 602	soldering land
203, 403, 603	solder

【Name of Document】 ABSTRACT OF THE DISCLOSURE

【Abstract】

【Object of the Invention】 It is an object to provide an electrode structure of a carrier substrate of a semiconductor device in which the strength and the reliability of the joint portion between an electrode of a semiconductor package and an electrode of a main substrate are improved.

【Means for solving the Problem】 A soldering land (103) that is an electrode of a carrier substrate (102) is hemispheric having a concentric hemispheric face hollow portion thereinside, a flange portion is provided in the circumferential portion thereof, and the outer diameter of the flange portion corresponds to the outer diameter of the conventional cylinder. Two slits (104) are provided in the flange portion and parts of a wall surface adjacent to the flange portion for venting air. A hemispheric face recess is provided in the carrier substrate (102) toward an outer surface, and the soldering land (103) is fixedly attached to the carrier substrate (102) so that the soldering land (103) is fitted into the recess and the flange portion abuts the outer surface of the carrier substrate.

【Selected Figure 】 Fig. 1